EFFECT OF TEMPERATURE IN THE DESIGN OF AN OPERATIONAL TRANSCONDUCTANCE AMPLIFIER BASED ON CNTFET

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ABSTRACT

In this paper we analyse the impact of temperature variations in the design of an Operational Transconductance Amplifier (OTA) based on CNTFET, where the active load is a cascode current sink mirror. In particular we determine the Voltage Transfer Characteristics (VTCs) and the Common Mode Rejection Ratio (CMRR) at different temperatures.

KEYWORDS

CNTFET, Modelling, Temperature Variations, OTA, Advanced Design System (ADS).

I. INTRODUCTION

Carbon NanoTube Field Effect Transistors (CNTFETs) are a new kind of molecular device, for which is possible to obtain good operation even at very high frequencies, as we shown in our previous papers [1-15].
In this paper we analyse the impact of temperature variations in the design of an Operational Transconductance Amplifier (OTA), determining the Voltage Transfer Characteristics (VTCs) and the Common Mode Rejection Ratio (CMRR) at different temperatures.
In the light of the results obtained we can say that the proposed circuit works with high CMRR and moderate gain values, which increase with temperature.

II. EFFECT OF TEMPERATURE IN THE DESIGN OF OTA

In the proposed design we consider the I-V model of CNTFET, already proposed by us in [5-6]. Therefore we suggest the reader to consult these References.
Regards to the C-V model, an exhaustive description of our C-V model, used in the proposed design, is widely described in [10] and also in this case the reader is requested to consult it.

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Moreover we considered a single wall n-CNTFETs with a diameter of 1.509 nm and 22 nm long in the ballistic transport hypothesis, for which in [16] we already shown the temperature variations on I-V characteristics.

The circuit of an Operational Transconductance Amplifier is reported in Fig. 1, where the active load is a cascode current sink mirror [17] working at 3 μA.

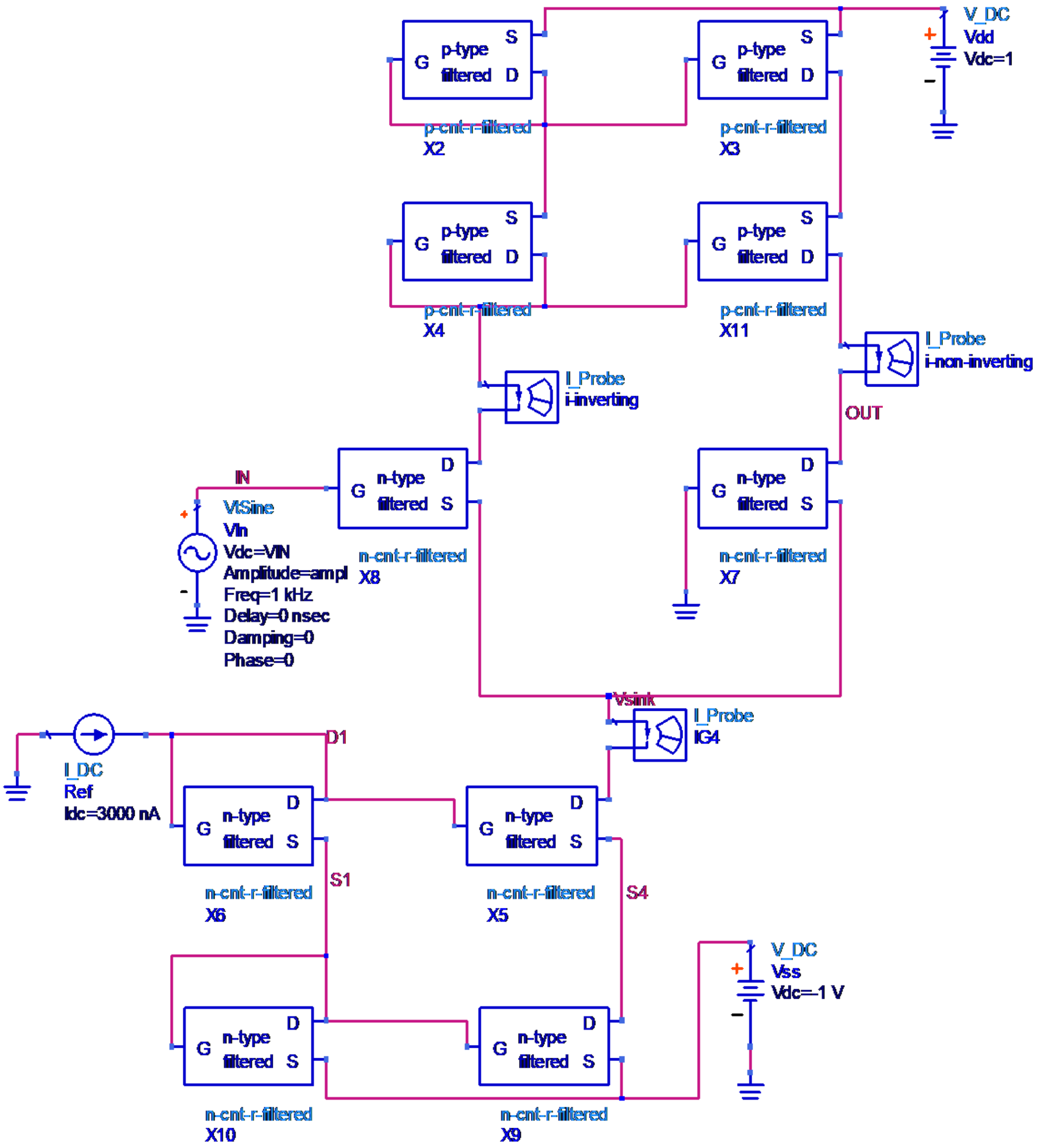

Figure 1. OTA circuit.

In particular, the developed OTA runs with 6 μW of power and also presents an high gain due to the cascode active load.

The Voltage Transfer Characteristics (VTCs) [18] at different temperatures are reported in Fig. 2, where it is easy to see the proposed OTA has not high gain at low temperatures (near 100 K) but can correctly operate at high temperatures.

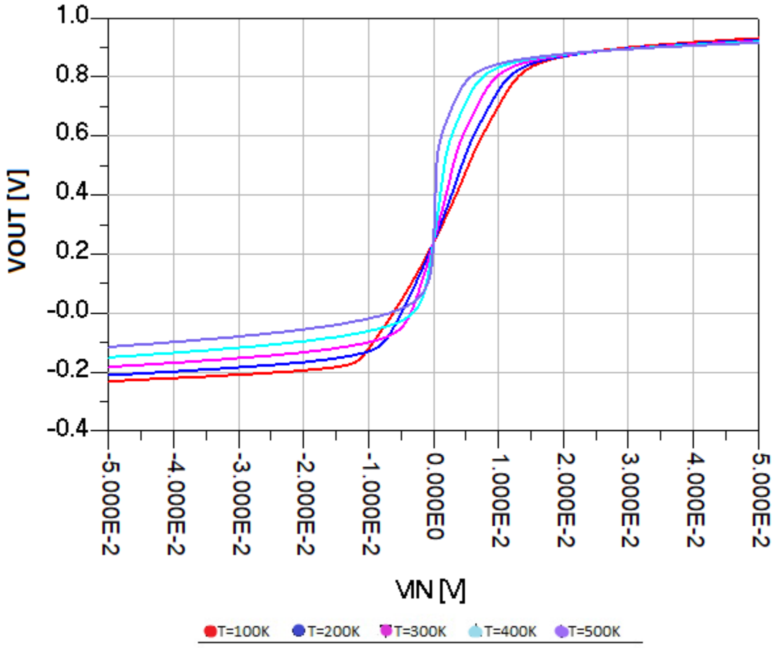

Figure 2. OTA VTCs vs temperature.

Moreover Fig. 2 shows the input and output dynamic in different environmental conditions. We have analysed the current splitting on the differential couple confirming them proper working and the result is shown in Fig. 3.

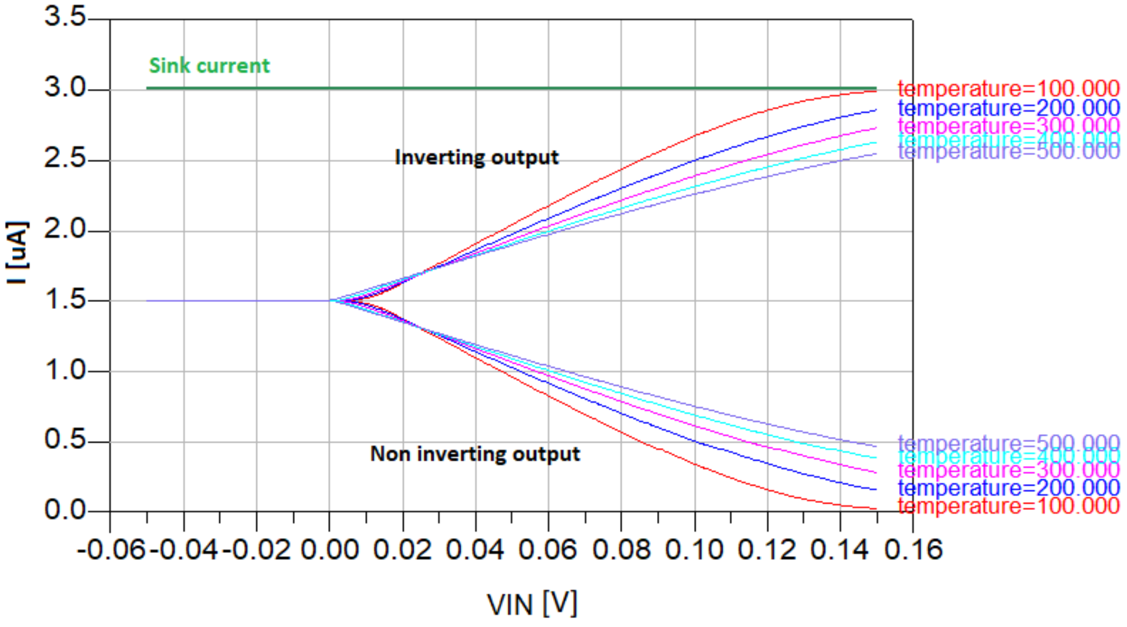

Figure 3. Differential couple with mirror active load current splitting.

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The total current sinking from the two branches of OTA, labelled "sink" in Fig. 3, has no visible dependence neither on input voltage nor on temperature. This is a positive check of the correct working of current mirror.

To determine the differential and common gain, at first we determined the differential gain directly from the VTC curves. Then, we have evaluated the common mode gain from the common mode transfer curves.

This procedure allows to evaluate the Common Mode Rejection Ratio (CMRR) [18], shown in Fig. 4, and amplifier gain, shown in Fig. 5 in different temperature conditions.

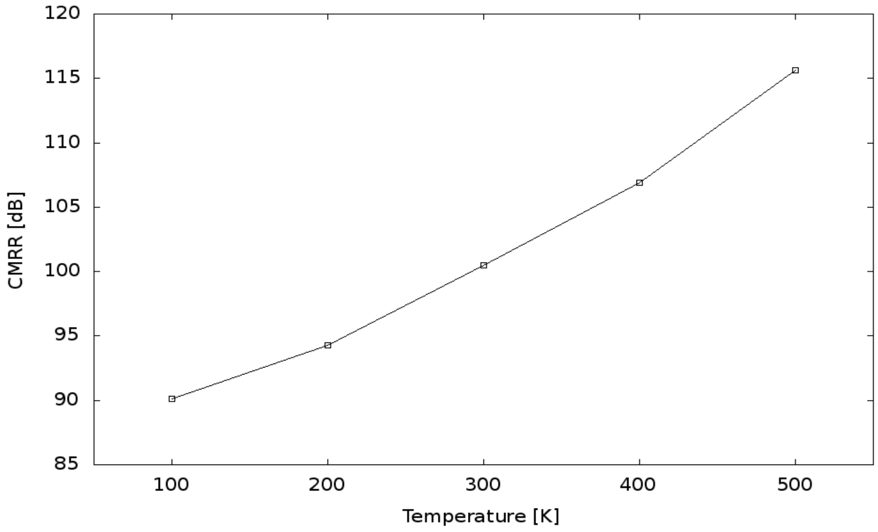

Figure 4. CMRR versus temperature.

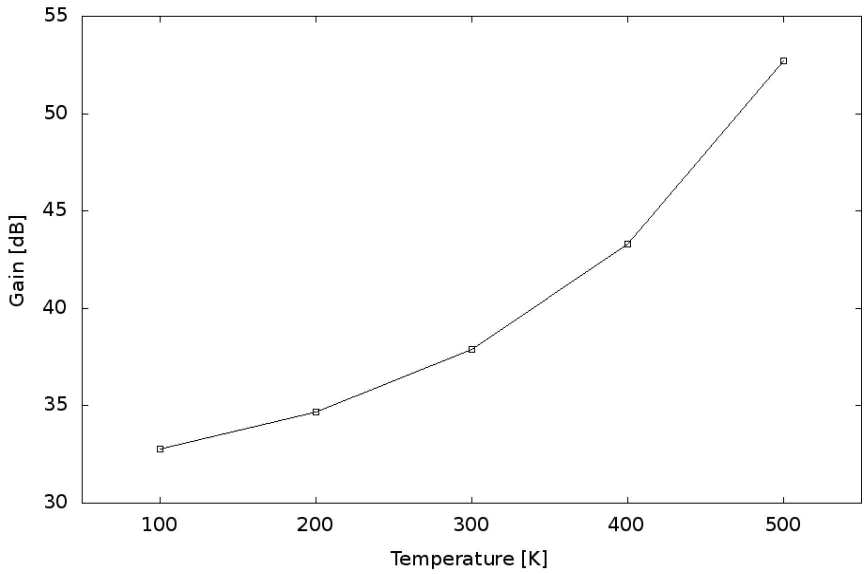

Figure 5. Amplifier gain vs temperature.

In the light of the results obtained we can say that proposed circuit works with high CMRR and moderate gain values, which increase with temperature.

Following the Allen-Holberg procedure [19], it has also been possible to determine the Input Common Mode Range (ICMR) of the proposed OTA at different temperatures.

The results are reported in Fig. 6.

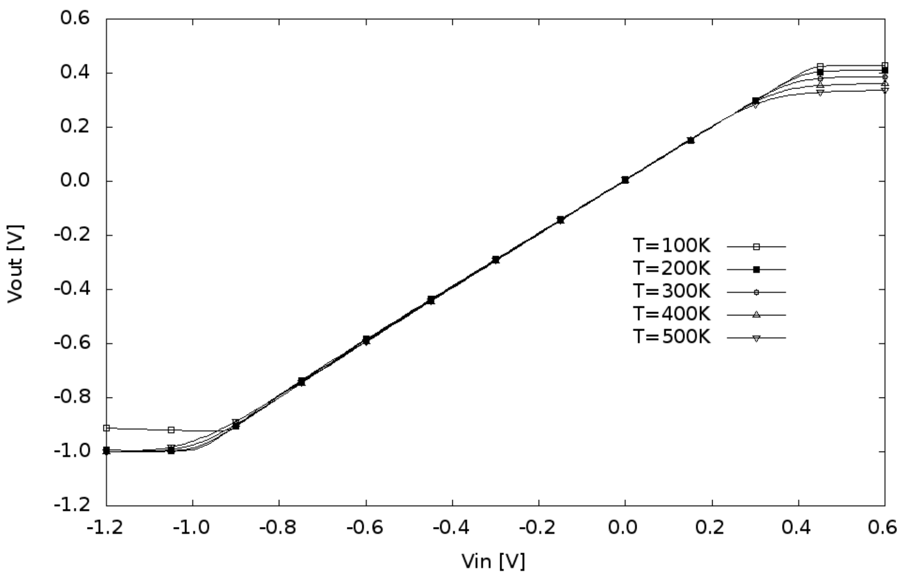

Figure 6. ICMR versus temperature.

In particular Fig. 6 shows that at T = 100 K the ICMR is (–0.9 V, 0.4 V) and at T = 500 K the ICMR is (–1.0 V, 0.2 V). Therefore we can affirm that the ICMR changes only slightly.

III. CONCLUSION AND FUTURE DEVELOPMENTS

In this paper we analysed the impact of temperature variations in the design of CNTFET-based OTA. In the proposed circuit we used a current mirror as an active load and we found a differential gain decreasing at lower temperature. We also noticed a common mode gain decreasing at high temperatures (caused by the mirror higher efficiency) resulting in a considerable CMRR increasing. However, OTA ICMR remains almost the same in all different conditions, proving that temperature slightly affects CNTFETs performance. All simulations have been obtained using ADS software [20].
Actually we are studying the effect of noise [21-23] in the CNTFET-based design of A/D circuits, and we are analyzing more thoroughly the effects of parasitic elements of interconnection lines in CNT embedded integrated circuits [24-25].

REFERENCES

[1] R. Marani, A. G. Perri: Il futuro della tecnologia: le nanotecnologie, *LA COMUNICAZIONE: NOTE, RECENSIONI & NOTIZIE*, Istituto Superiore delle Comunicazioni e delle Tecnologie dell'Informazione, Rome, **LVI**, ISSN: 1590-864X, 169 – 178, (2009).
[2] A. G. Perri: *Dispositivi Elettronici Avanzati*, Progedit Editor, Bari, Italy; ISBN: 978-88-6194-081-9, (2018).
[3] A.G. Perri, R. Marani: *CNTFET Electronics: Design Principles*, Progedit Editor, Bari, Italy, ISBN: 978-88-6194-307-0, (2017).
[4] A. G. Perri: *Modelling and Simulations in Electronic and Optoelectronic Engineering*, Research Signpost, Kerata, ISBN: 978-81-308-0450-7, (2011).
[5] G. Gelao, R. Marani, R. Diana, A.G. Perri: A Semi-Empirical SPICE Model for n-type Conventional CNTFETs, *IEEE Transactions on Nanotechnology*, **10**(3), 506-512, (2011).
[6] R. Marani, A.G. Perri: A Compact, Semi-empirical Model of Carbon Nanotube Field Effect Transistors oriented to Simulation Software, *Current Nanoscience*, **7**(2), 245-253, (2011).
[7] R. Marani, A.G. Perri: Simulation of CNTFET Digital Circuits: a Verilog-A Implementation, *International Journal of Research and Reviews in Applied Sciences*, **11**(1), 74-81, (2012).
[8] R. Marani, A.G. Perri: Modelling and Implementation of Subthreshold Currents in Schottky Barrier CNTFETs for Digital Applications, *International Journal of Research and Reviews in Applied Sciences*, **11**(3), 377-385, (2012).
[9] R. Marani, G. Gelao, A.G. Perri: Comparison of ABM SPICE library with Verilog-A for Compact CNTFET model implementation, *Current Nanoscience*, **8**(4), 556-565, (2012).

[10] R. Marani, G. Gelao, A.G. Perri: Modelling of Carbon Nanotube Field Effect Transistors oriented to SPICE software for A/D circuit design, *Microelectronics Journal*, **44**(1), 33-39, (2013).
[11] R. Marani, A.G. Perri: Analysis of CNTFETs Operating in SubThreshold Region for Low Power Digital Applications, *ECS Journal of Solid State Science and Technology*, 5(2), M1-M4, (2016).
[12] G. Gelao, R. Marani, L. Pizzulli, A.G. Perri: A Model to Improve Analysis of CNTFET Logic Gates in Verilog-A-Part I: Static Analysis, *Current Nanoscience*, **11**(4), 515-526, (2015).
[13] G. Gelao, R. Marani, L. Pizzulli, A.G. Perri: A Model to Improve Analysis of CNTFET Logic Gates in Verilog-A-Part I: Dynamic Analysis, *Current Nanoscience*, **11**(6), p. 770-783, (2015).
[14] R. Marani, A.G. Perri: A Simulation Study of Analogue and Logic Circuits with CNTFETs, *ECS Journal of Solid State Science and Technology*, **5**(6), M38-M43, (2016).
[15] R. Marani, A.G. Perri: A Comparison of CNTFET Models through the Design of a SRAM Cell, *ECS Journal of Solid State Science and Technology*, **5**(10), M118-M1, (2016).
[16] R. Marani, A.G. Perri: Impact of Temperature Variations on Design Parameters of CNTFET, *International Journal of Advances in Engineering & Technology (IJAET)*, **14**(4), 44-51, (2021).
[17] R. Marani, A.G. Perri: A Comparative Study of CNTFET and MOSFET Devices through the Design of Current Mirrors, *International Journal of Advances in Engineering & Technology (IJAET)*, **13**(4), 116-122, (2020).
[18] A.G. Perri: "*Fondamenti di Elettronica"*, Ed. Progedit, Bari, Italy, (2009).
[19] P.E. Allen, D.R. Holberg: *CMOS Analog Circuit Design*, Oxford University Press, (2013).
[20] Verilog-AMS language reference manual, Version 2.2, (2014).
[21] R. Marani, G. Gelao, A.G. Perri: A Compact Noise Model for C-CNTFETs, *ECS Journal of Solid State Science and Technology*, **6**(4), pp. M118–M126, (2017).
[22] R. Marani, A.G. Perri: Comparative analysis of noise in current mirror circuits based on CNTFET and MOS Devices, *International Journal of Nanoscience and Nanotechnology*, **17**(2), 121-129, (2021).
[23] R. Marani, A.G. Perri: A Simulation Study of Noise Behavior in Basic Current Mirror using CNTFET and MOSFET, *International Journal of Emerging Technology and Advanced Engineering*, **11**(7), 13-18, (2021).
[24] R. Marani, A.G. Perri: Effects of Parasitic Elements of Interconnection Lines in CNT Embedded Integrated Circuits, *ECS Journal of Solid State Science and Technology*, **9** (2020).
[25] R. Marani, A.G. Perri: A Procedure to Analyze a CNTFET-based NOT gate with Parasitic Elements of Interconnection Lines", *International Journal of Nanoscience and Nanotechnology*, **17)**3), 161-171, (2021).

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