PERFORMANCE OF HYBRID REACTIVE POWER COMPENSATORS IN A MULTI-TERMINAL HVDC TRANSMISSION SYSTEM FEEDING WEAK AC NETWORKS DURING TRANSIENT FAULT CONDITIONS

S. Singaravelu, S. Seenivasan
Department of Electrical Engineering,
Annamalai University, Annamalainagar-608002, Tamilnadu, India

ABSTRACT
In this paper performance analysis of various hybrid reactive power compensators (RPC's) at the inverter AC sides of a line commutated converter (LCC) based multi-terminal HVDC (MTDC) transmission system, feeding weak AC networks, is carried out to thoroughly gather the mechanisms of interactions between an HVDC system and weak AC systems. The hybrid compensator is realized by equally mixing the fixed capacitor (FC) with any one of the following compensators: synchronous compensator (SC); static var compensator (SVC); static synchronous compensator (STATCOM). The HVDC transmission system model is simulated using Matlab with firefly algorithm based optimal proportional integral (PI) controller for rectifiers and inverters control. The performances of hybrid RPC's (FC+SC, FC+SVC and FC+STATCOM) are investigated during various transient fault conditions and the results are compared with the performance of the SC, SVC and STATCOM to focus the supremacy of the hybrid compensators. The simulation results authorize that the equal combination of FC and STATCOM has a steady and fastest response. The outcomes also demonstrate the superiority of the firefly algorithm based optimal PI controller over the conventional PI controller. The harmonic existing in the inverter AC side is also observed under steady state operation to ascertain the quality of power supply.

KEYWORDS: *Firefly algorithm, Hybrid RPC's, MTDC, PI controller, Weak AC system.*

I. INTRODUCTION

The MTDC power transmission technology delivers numerous advantages such as rapid rises in the power carrying capacity, flexibility in power control and the possibility of connecting new offshore load/generation terminal [1], [2],[3]. During occurrence of the fault, in the MTDC system without appropriate control and protection, the fault at one terminal will affect the interconnected terminals. Under such circumstances of the MTDC system, by presuming that the blocking of the converter is successful, special control and protection is offered. On the other hand, this assumption is not necessarily valid in terms of the practical operation of converters in the HVDC system such as
1) During the communication outage of control signals, the whole converter can be out of control and cannot be blocked, 2) A most common circumstance is that one of the six pulse converter arm is given out to be blocked [4], [5], [6]. Hence, it is worth identifying the possible hazard to the MTDC system by spreading the fault at one terminal without closing up the converters.
Further, the conduct of the HVDC system plays ever greater roles in the functioning of entire AC/DC power systems. It is essential to understand the mechanisms of the interactions between an HVDC system and an AC network so the HVDC system can be operated in a manner that enriches the stability of the entire power grid. The significance of this interaction [7] largely depends on the strength of the AC system at the converter bus, which is presented by the short circuit ratio (SCR). The following SCR values [8] can be applied to classify AC systems: a) SCR >3 for a strong system, b) $2 \leq SCR < 3$ for a weak system, c) $SCR < 2$ for a very weak organization. Numerous works have

been used to identify the interaction between AC networks and HVDC systems. The voltage stability associated phenomena [9] in a monopolar HVDC terminal feeding weak AC network and solutions for eradicating the risks of potential collapse and for evading control induced oscillations were discussed. The Nelson River monopolar HVDC system with new synchronous compensators is analyzed in [10] and also highlighted planning requirements and synchronous compensators specification to optimize power delivery by the DC links. An analysis of the dynamic performance of monopolar HVDC systems [11] connected to a weak AC system is carried out for various exciter characteristics of synchronous machines connected to the converter bus. The direct transient stability margin (TSM) prediction method [12] based on the extended equal area criterion is used for the integration of the monopolar HVDC transmission system and SVC into the power system. The usage of STATCOM at the inverter end of a classical monopolar HVDC system for the reactive power support is considered in [13]. The coordination between STATCOM and monopolar HVDC classic link feeding a weak AC network is examined in [14] with two different control technique during various fault conditions.

Analysis of the fault recovery performance and suppression of dynamic overvoltage (DOV) criterion of a monopolar HVDC system feeding a weak AC network [15] is carried out with a FC, SC, thyristor controlled reactor (TCR), thyristor switched capacitor (TSC), metal oxide varistor (MOV), series capacitor device (SCD). The DC power recovery and suppression of temporary overvoltage (TOV) of a monopolar HVDC system feeding a very weak AC network [16], [17] have been discussed. In order to make the analysis complete, it is highly essential to consider the suppression of TOV and fault recovery for an HVDC system feeding a weak AC network. Therefore, in [18] simulation of both the fault recovery performance as well as suppression of TOV during various transient fault conditions has been carried out for a monopolar HVDC system connected to a weak AC network with the hybrid RPC's: FC+SC, FC+SVC and FC+STATCOM. As an addition, in this paper, the detailed simulation study carried out in monopolar HVDC system is extended to a multi-terminal HVDC system by analyzing the DC power recovery performance and suppression of TOV during various transient fault conditions. The harmonic investigation is also carried out under steady state to assure the quality of power supply on inverter AC sides.

The conventional PI controller used for rectifier and inverter controllers of HVDC system causes instability due to deficiency in tuning its gain during abnormal conditions. To overcome this drawback intelligent technique [19], [20], [21], [22], are introduced for proper tuning of the PI controller parameters. Yet, in all those tuning methods the principal signals used to fix the PI gains of the rectifier and the inverter current controllers are current error and its derivative. For the inverter gamma controller, the gamma error and its derivative are used. In this paper, minimization of the rectifier and the inverter DC power errors are considered as an objective function which is achieved by the firefly optimization algorithm, to fix the PI gains of the respective PI controller. To demonstrate the effectiveness of firefly algorithm based optimal PI controller, on transient performance, it has been compared with conventional PI controller.

The rest of the paper is organized as follows: section II addresses the model of LCC-HVDC transmission system. Section III describes the application of firefly algorithm for obtaining optimal gain values for PI controllers. Section IV details our simulation results and discussion. Finally conclusions are given in section V.

II. MODELLING OF MULTI-TERMINAL HVDC TRANSMISSION SYSTEM

A LCC based four-terminal HVDC system feeding two strong AC networks is presented in [23], in which inverter side AC networks are replaced by weak AC networks as shown in the Figure 1. Each rectifier side AC system of 500kV, 5000MVA, 60Hz is connected to each inverter side AC system of 345kV, 2500MVA, 50Hz through an HVDC network. Generally, the AC system is represented by damped LLR equivalents. The Passive filters of 450MVAr are connected on the source side to eliminate the 11^{th} and 13^{th} (the double tuned type) order and above 24^{th} (second order high pass filter) order current harmonics and synchronous or static compensator or fixed capacitor with synchronous or static compensator is used (150MVAr) for reactive power compensation. Each rectifier and inverter is 12-pulse converters. The DC network model consists of a smoothing reactor for the rectifier and the inverter bridges, a passive filter of double tuned type to mitigate the 12^{th} and 24^{th}

order DC voltage harmonics and the DC line. The DC link of 1500 km is modelled as a distributed parameter line model with lumped losses. Each rectifier is equipped with a current controller to maintain the DC system current constant. Each inverter is provided with a current controller to maintain the DC system current constant and a constant extinction angle or gamma controller. The reference current for the current controllers is obtained from the master controller output through the voltage dependent current order limiter (VDCOL). In order to protect each rectifier and each inverter DC protection functions are implemented in each converter. In the inverter side AC network, the following six reactive power compensator options is studied.

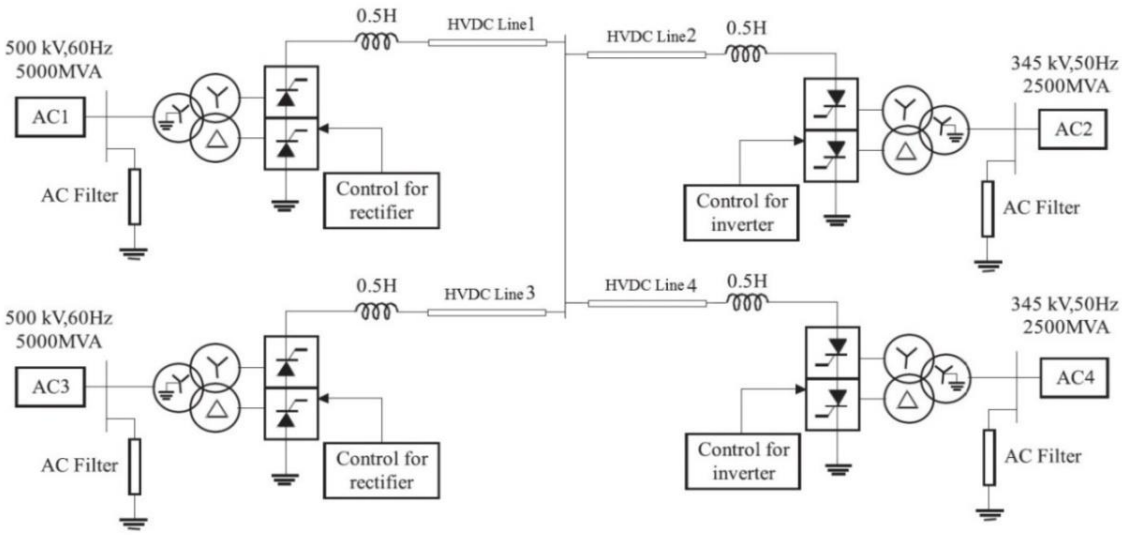
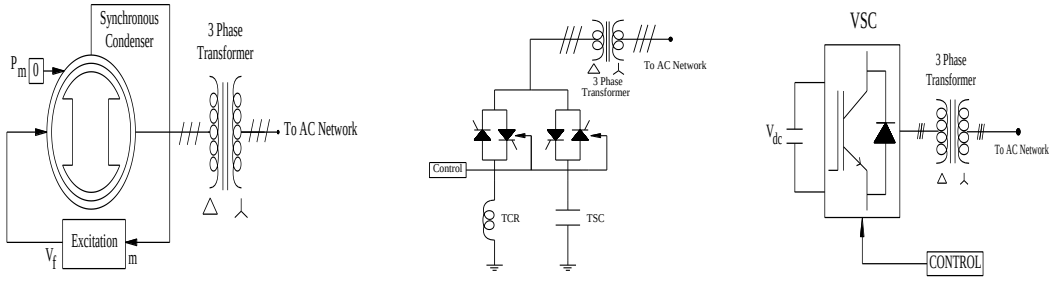


Figure 1. Four-Terminal HVDC transmission system model feeding weak AC networks.



(a) SC (b) SVC (c) STATCOM

Figure 2. Schematic of RPC's.

2.1. Synchronous Compensator

The SC model of 150MVAr shown in Figure 2 (a) is represented with the simplified synchronous machine block which models, both the electrical and mechanical characteristics of a simple synchronous machine. The SC uses the solid static excitation system.

2.2. Static Var Compensator

A 150MVAr SVC shown in Figure 2 (b) regulates voltage on a 345kV system. The SVC consists of a 345kV/16kV, 168MVA coupling transformer, one 60MVAr TCR bank and one 180MVAr TSC connected to the secondary side of the transformer. Switching the TSC in and out allows a continuous variation of the secondary reactive power from zero to 180MVAr capacitive, whereas phase control of the TCR allows a continuous variation from zero to 60MVAr inductive.

2.3. Static Synchronous Compensator

The STATCOM shown in Figure 2 (c) is located at the inverter side of the HVDC link and has a rating of ±150MVAr. This STATCOM is a typical simple PWM voltage source converter (VSC). It

consists of a 6 pulse VSC inverter and a series connected capacitors which act as a variable DC voltage source. Based on a VSC, the STATCOM regulates system voltage by absorbing or generating reactive power.

2.4. An Equal Mix of FC and SC

The FC (75MVAr) and SC (75MVAr) are connected to the inverter bus in this scheme. In steady state the FC and SC each supply 75MVAr.

2.5. An Equal Mix of FC and SVC

The FC (75MVAr) and SVC (-90MVAr, +30MVAr) are connected to the inverter bus in this scheme. In steady state the FC and SVC each supply 75MVAr.

2.6. An Equal Mix of FC and STATCOM

The FC (75MVAr) and STATCOM (±75MVAr) are connected to the inverter bus in this scheme. In steady state the FC and STATCOM each supply 75MVAr.

III. APPLICATION OF FIREFLY ALGORITHM FOR OBTAINING OPTIMAL GAIN VALUES FOR PI CONTROLLERS

In this paper, optimization of the rectifier and the inverter side DC power error is picked as a prime objective function which has to be minimized. To achieve the same DC power (P_{DCMEA}) and its reference (P_{DCREF}) is compared to get the error signal. The integral square error of the rectifier DC power error and inverter DC power error are controlled by the firefly algorithm [24], [25], [26], [27], to fix the gain of the rectifier current PI controller and to fix the gain of the both inverter current PI controller and the gamma PI controller respectively. This approach guarantees the reduced computational procedure, faster recovery and reduced TOV. The schematic diagram of the firefly algorithm based tuning technique is shown in Figure 3. The general flow chart for minimization of the rectifier/ the inverter DC power error function using firefly algorithm is shown in Figure 4.

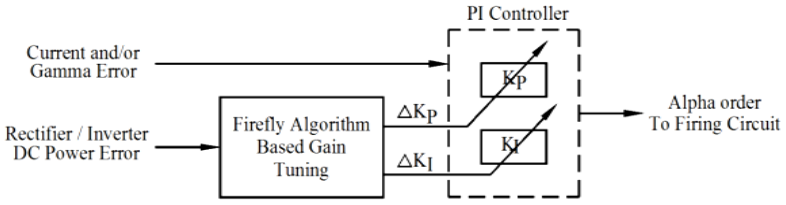


Figure 3. Schematic diagram of the firefly algorithm based tuning technique.

IV. SIMULATION RESULTS AND DISCUSSION

In order to know the interaction between AC network and HVDC systems, the simulation model is implemented in Matlab based on the data [28]. At the inverter AC Side, SC, SVC, STATCOM, FC+SC, FC+SVC and FC+STATCOM are the various RPC's considered for investigation. In all the cases steady state AC voltage and current waveforms at the inverter AC side and their harmonic spectrums are observed to study the quality of the AC supply. The transient performance of the HVDC system is analyzed in the presence of various RPC'S for a duration of two seconds under various fault conditions to study the suppression of TOV and fault recovery. For the purposes of comparison, identical fault duration of 0.05seconds was used for all types of faults.

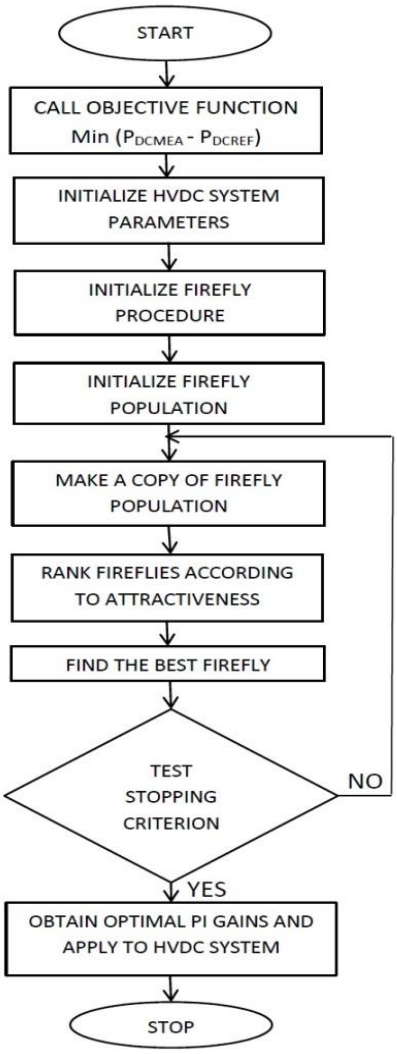


Figure 4. Flowchart for minimization of the rectifier/the inverter DC power error function using firefly algorithm.

During the transient performance analysis the following cases are considered: (1) Fault at rectifier station 1 and their impact on inverter station 1 and 2, (2) Fault at inverter station 1 and their impact on inverter station 1 and 2. Since the rectifier 1 and 2 and inverter 1 and 2 are identical in the system under study discussion is limited to the cases mentioned above. The inverter side RMS AC voltage waveforms are observed during various AC faults and DC fault on the rectifier side to study the TOV suppression capability of the proposed firefly algorithm based PI controller. In order to analyze the fault recovery capability with the proposed firefly algorithm based PI controller, the inverter DC power waveforms are observed, under various AC faults and DC faults at rectifier and inverter side. In all the cases, the TOV suppression and fault clearance capability of the firefly algorithm based PI controller are compared with conventional PI controller of an HVDC transmission system.

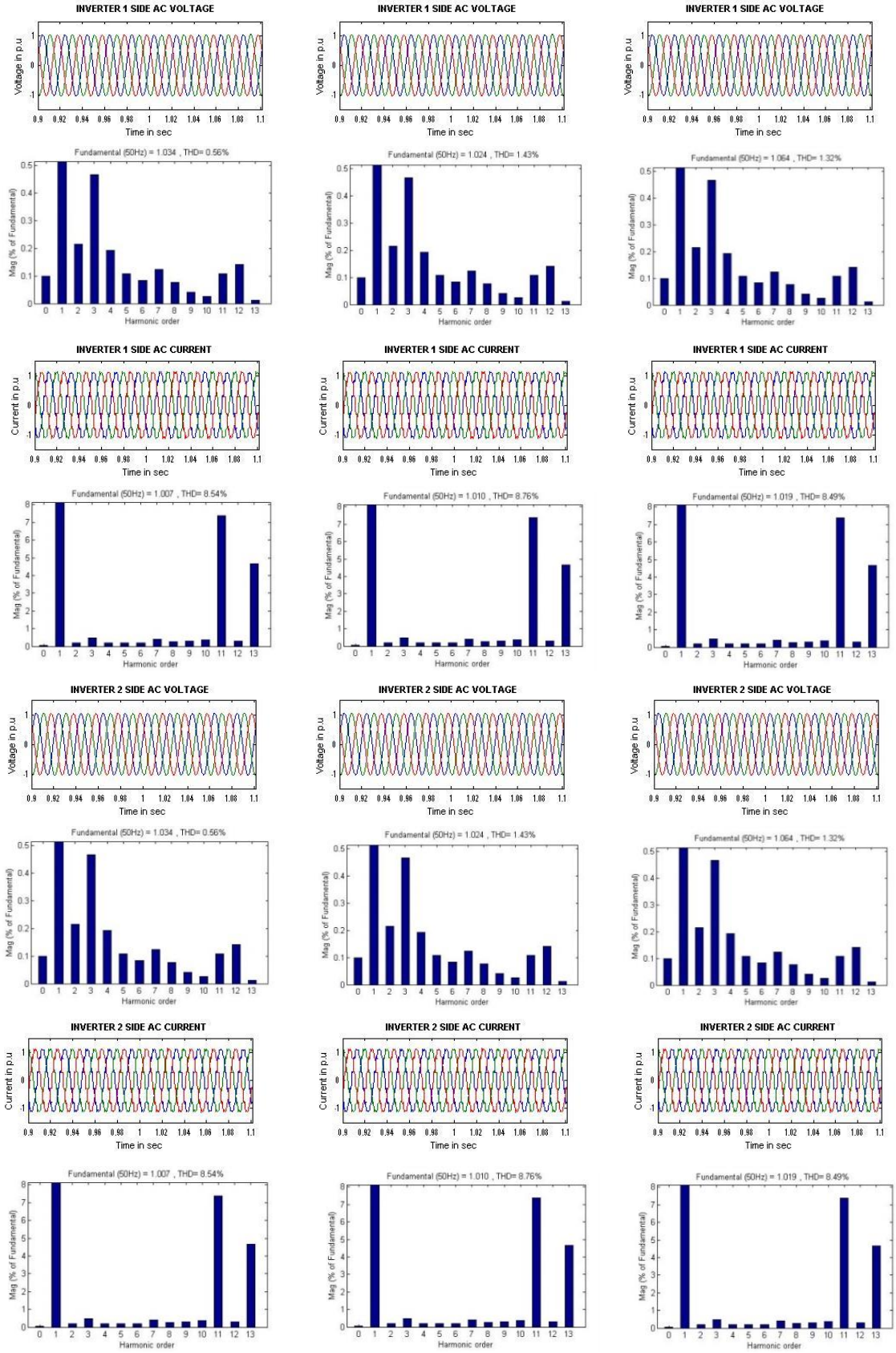


Figure 5. Inverter 1 and 2 side AC waveforms and their harmonic spectrums during steady state operation -with SC (Left), -with SVC (Middle), -with STATCOM (Right).

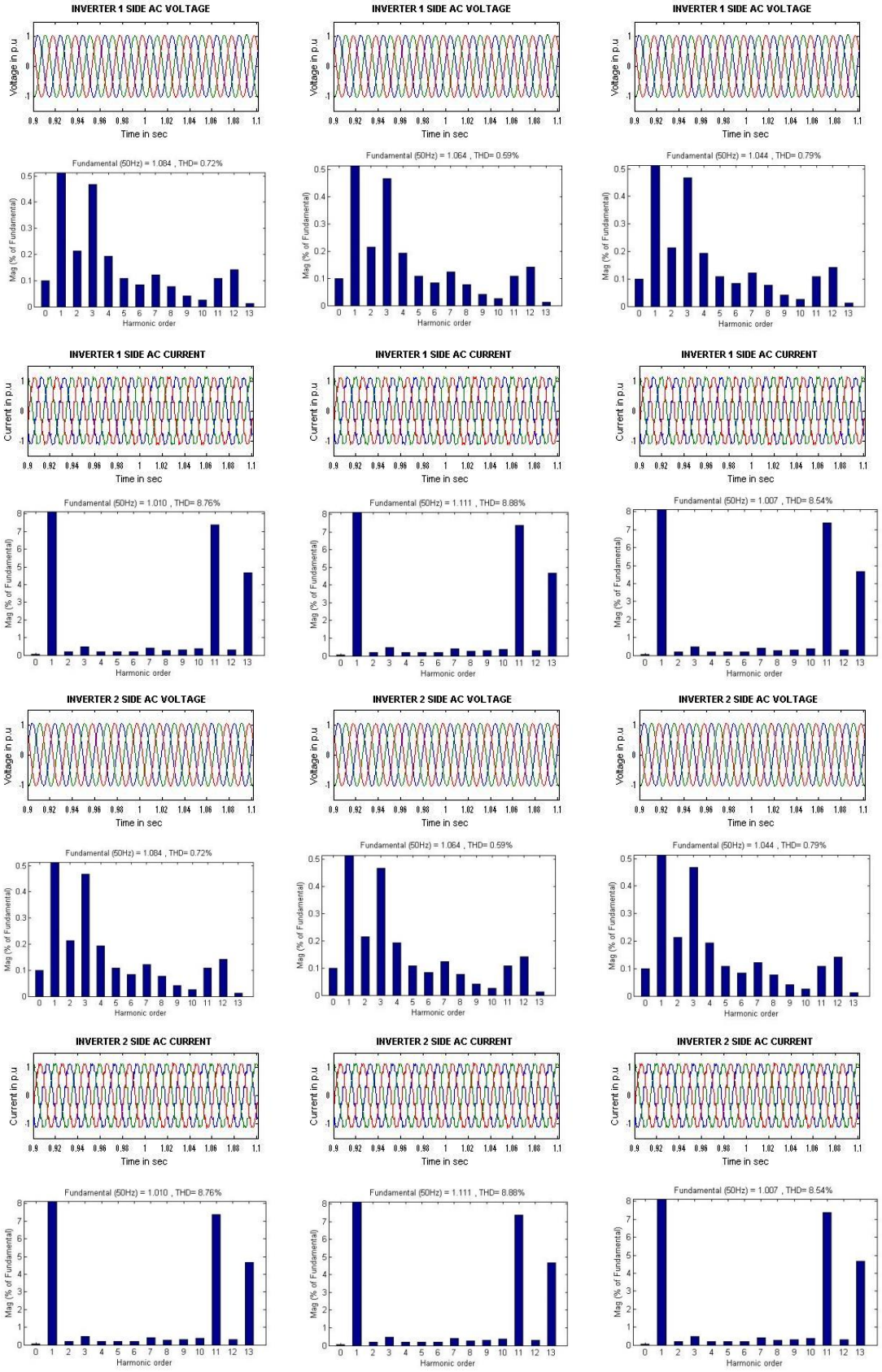


Figure 6. Inverter 1 and 2 side AC waveforms and their harmonic spectrums during steady state operation -with FC+SC (Left), -with FC+SVC (Middle), -with FC+STATCOM (Right).

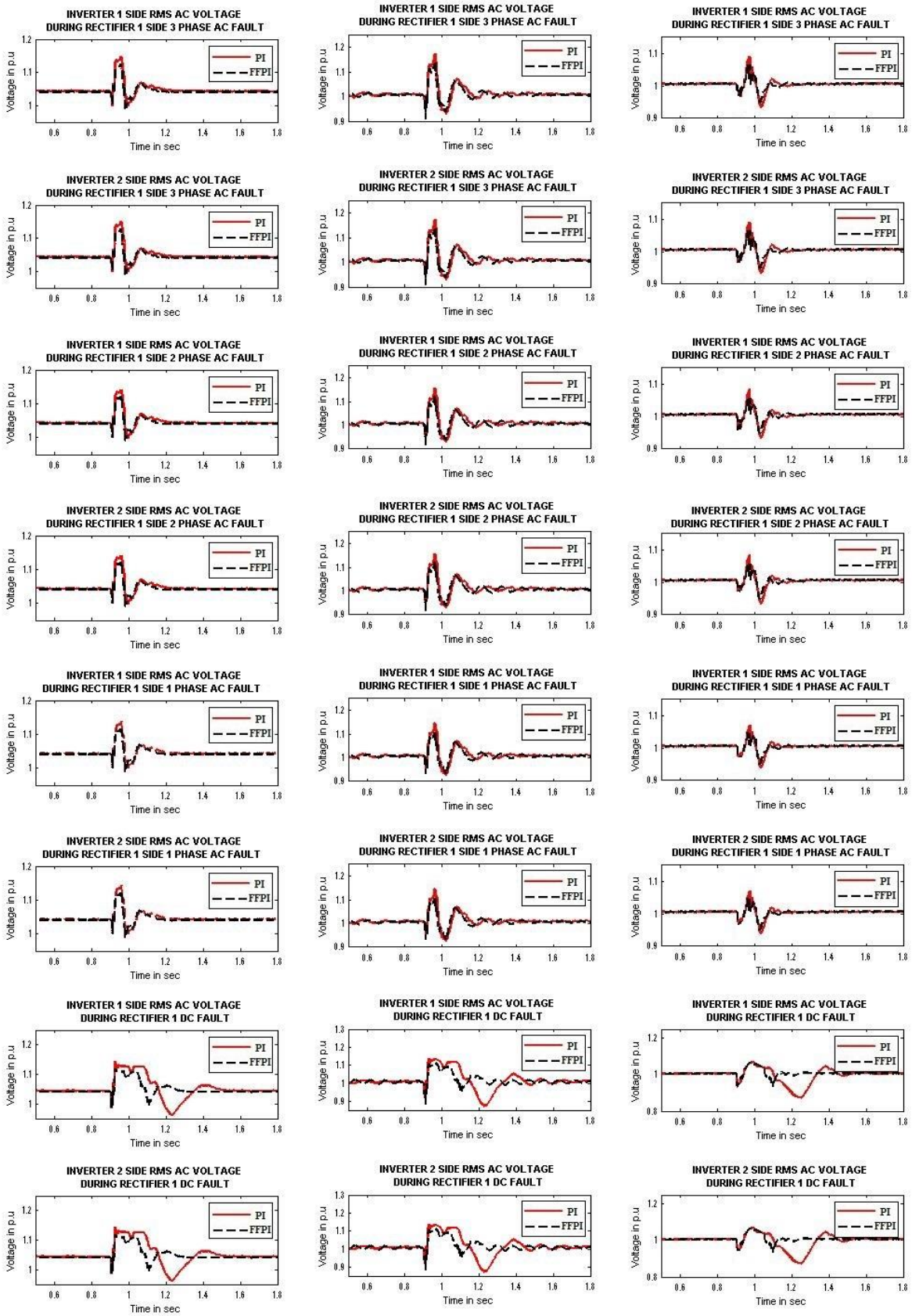


Figure 7. Inverter 1 and 2 AC bus RMS voltage when disturbances occur on the DC line or at the rectifier side - with SC (Left), -with SVC (Middle), -with STATCOM (Right).

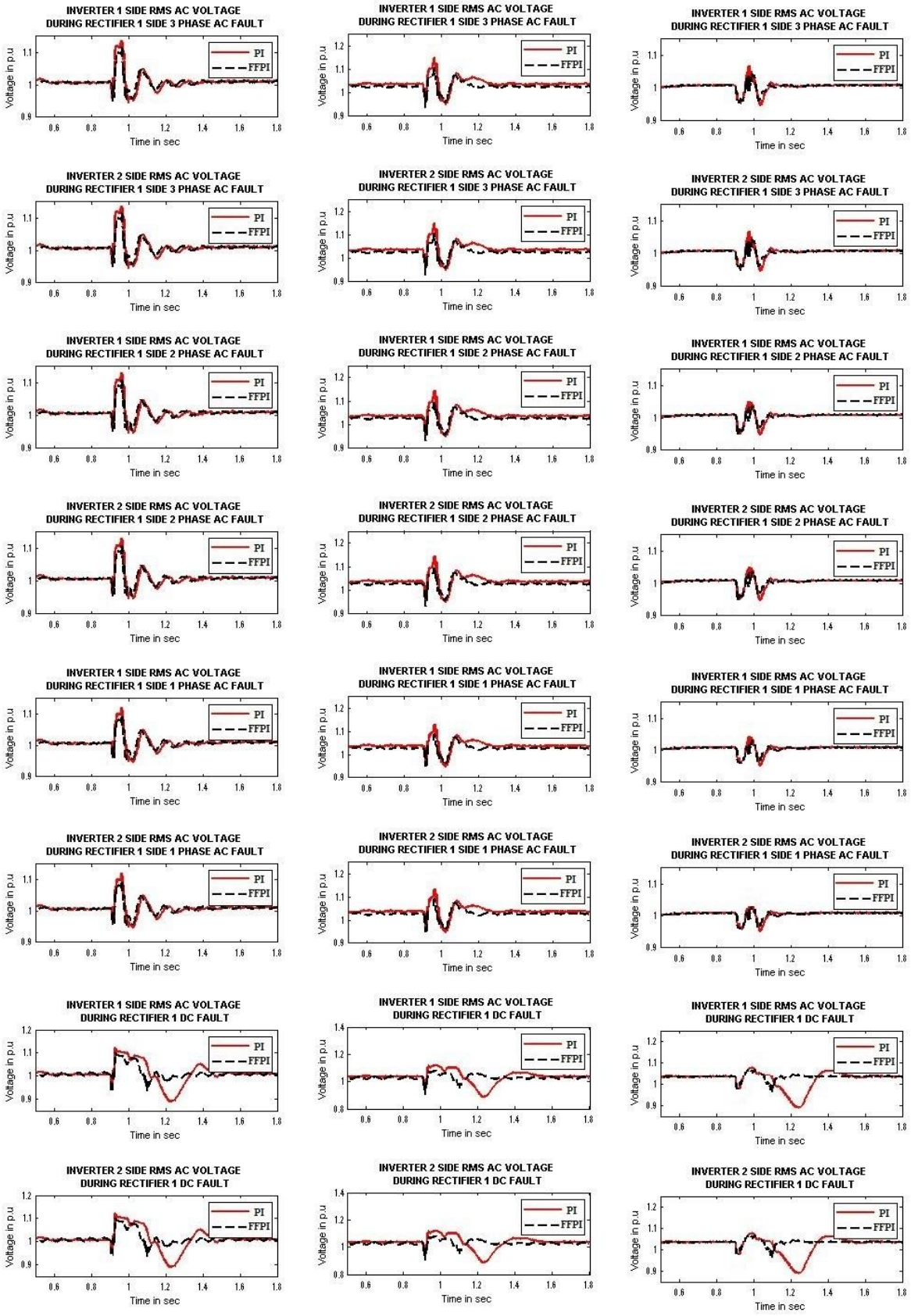


Figure 8. Inverter 1and 2 AC bus RMS voltage when disturbances occur on the DC line or at the rectifier side - with FC+SC (Left), -with FC+ SVC (Middle), -with FC+STATCOM (Right).

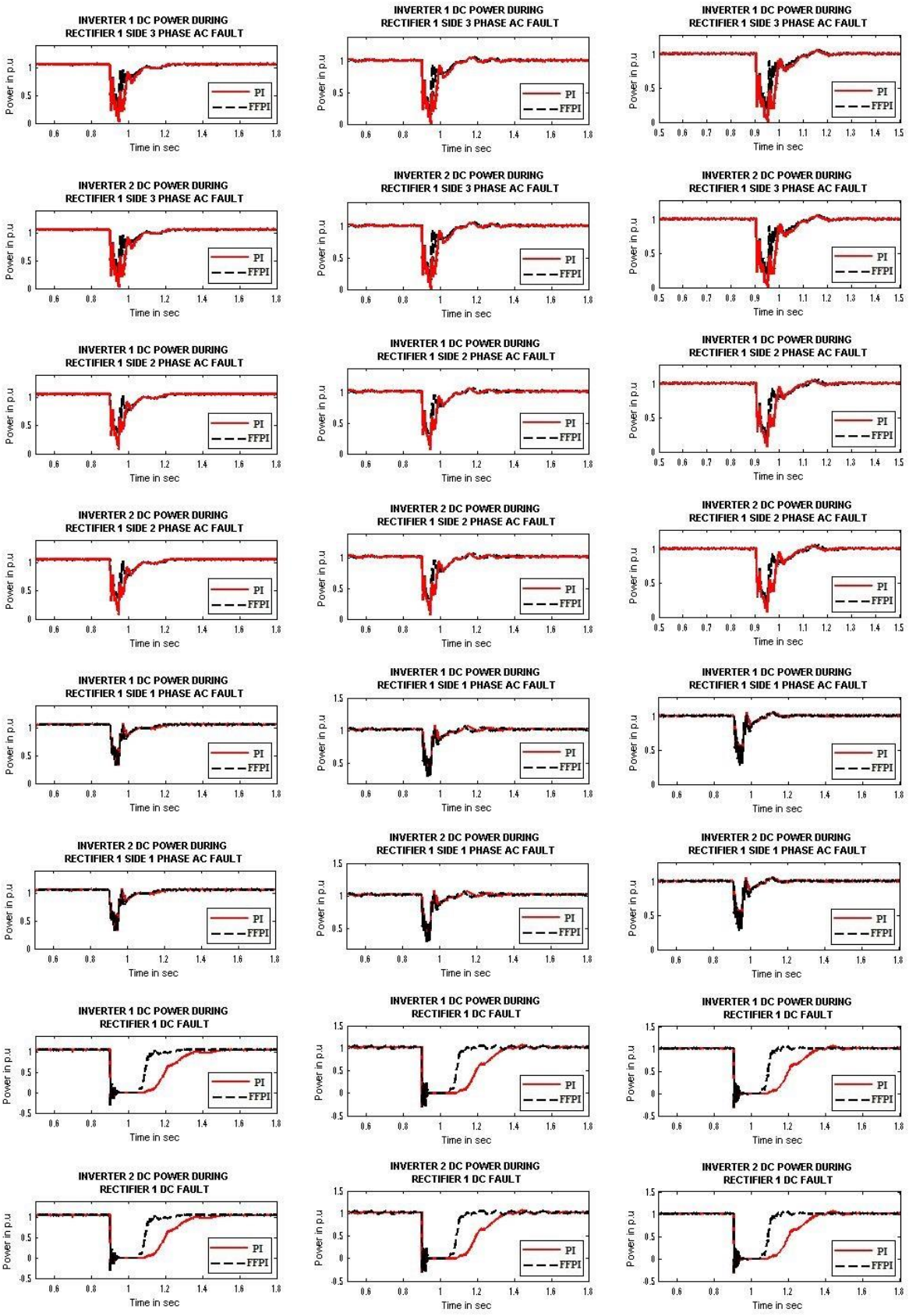


Figure 9. Inverter 1 and 2 DC power when AC and DC disturbances occur on the rectifier side -with SC (Left), -with SVC (Middle), -with STATCOM (Right).

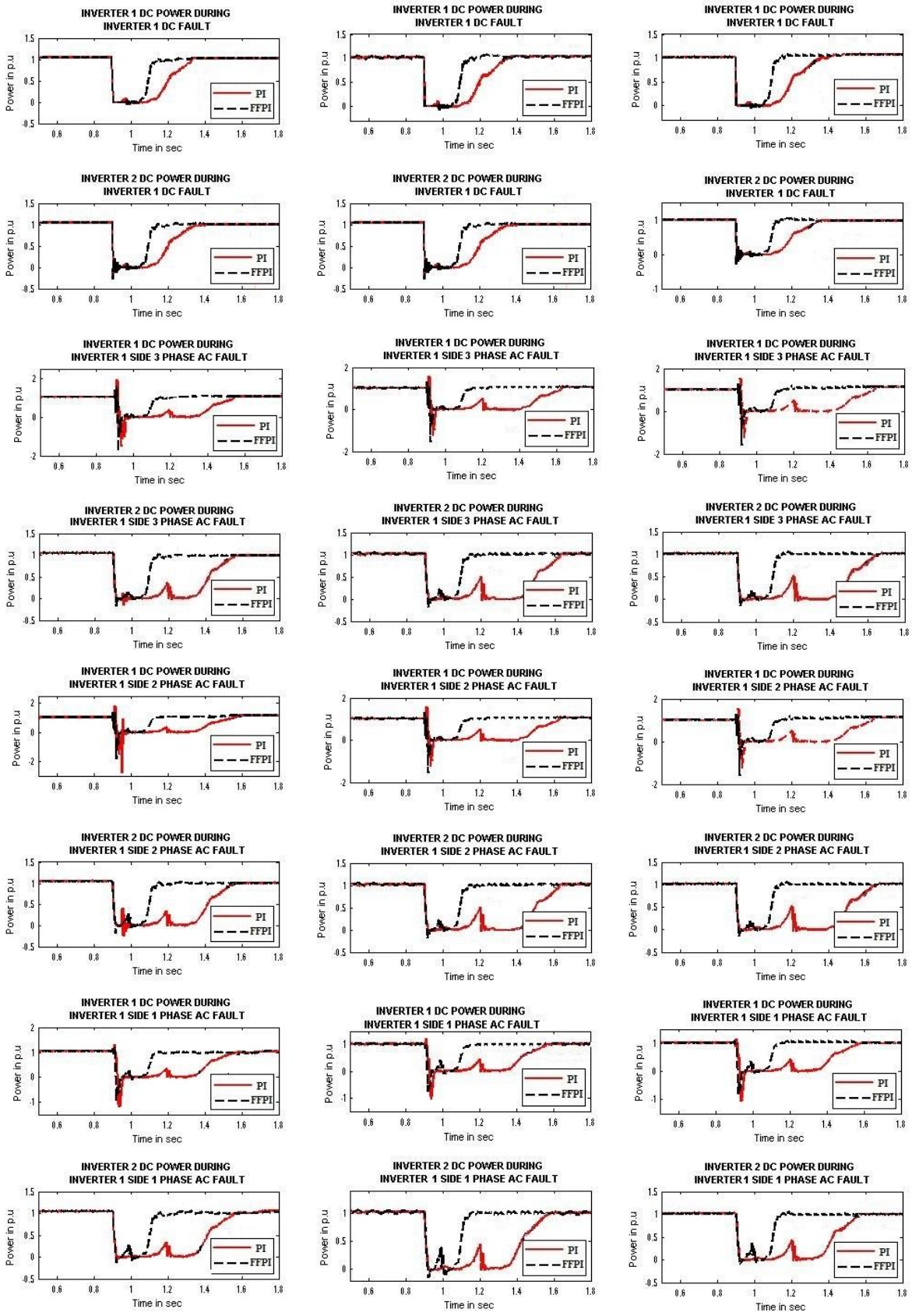


Figure 10. Inverter 1 and 2 DC power when AC and DC disturbances occur on the inverter side -with SC (Left), -with SVC (Middle), -with STATCOM (Right).

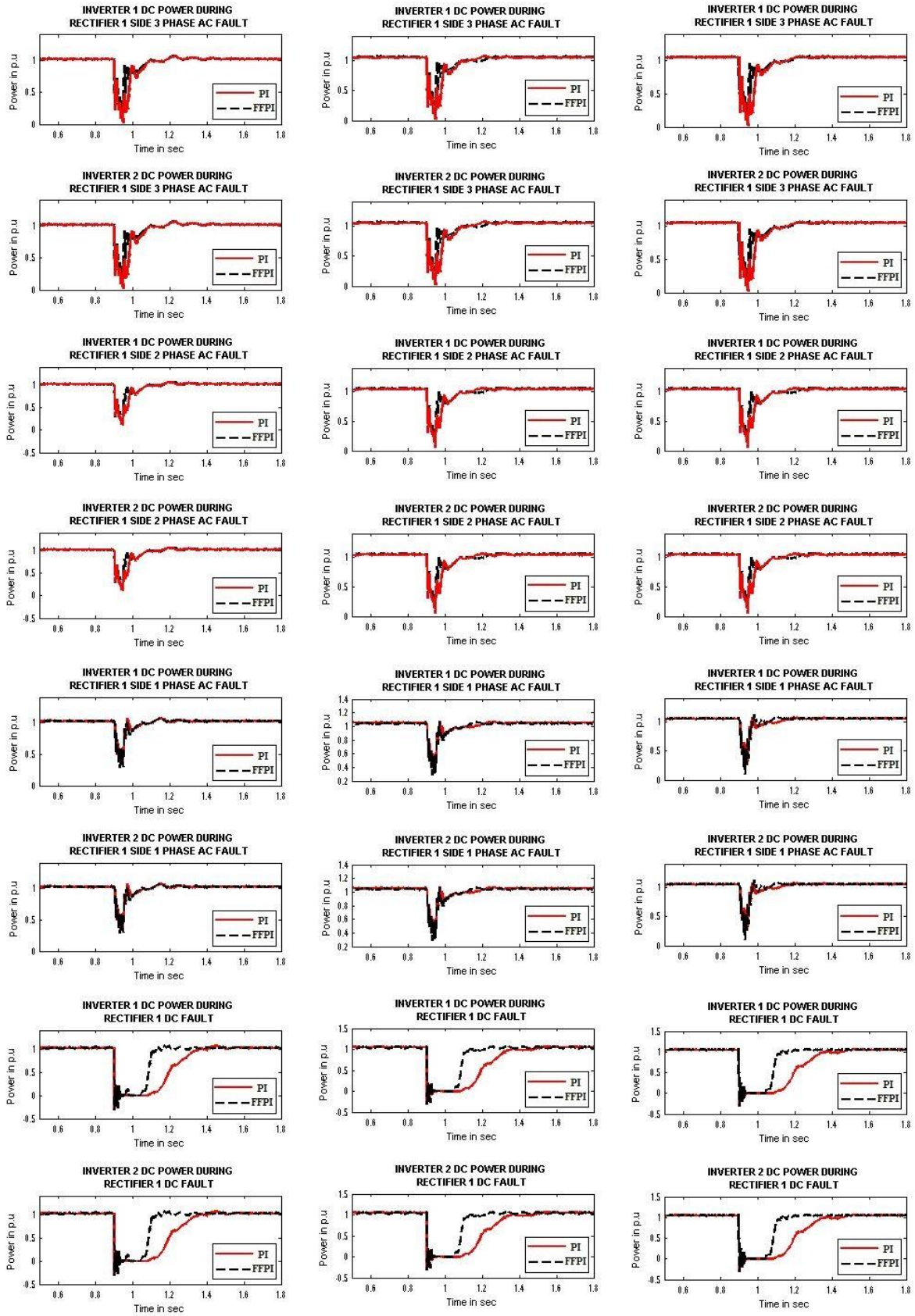


Figure 11. Inverter 1 and 2 DC power when AC and DC disturbances occur on the rectifier side -with FC+SC (Left), -with FC+SVC (Middle), -with FC+STATCOM (Right).

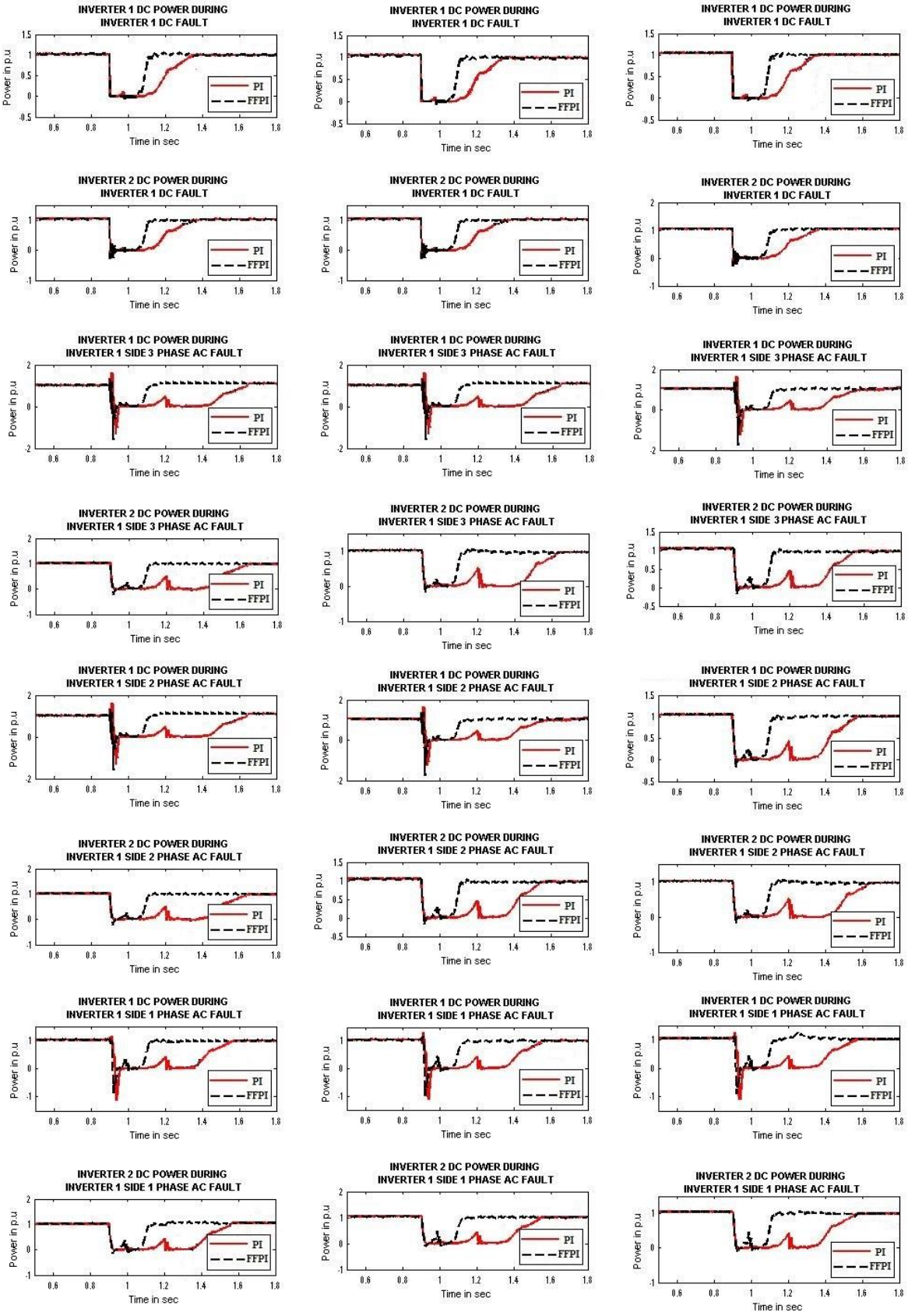


Figure 12. Inverter 1 and 2 DC power when AC and DC disturbances occur on the inverter side -with FC+SC (Left), -with FC+SVC (Middle), -with FC+STATCOM (Right).

Table 1. Harmonics present in the inverter side AC quantities.

% AC Harmonics for various RPC's		SC	SVC	STATCOM	FC+SC	FC+SVC	FC+ STATCOM
Voltage	Inverter 1	0.56	1.43	1.32	0.72	0.59	0.79
	Inverter 2	0.56	1.43	1.32	0.72	0.59	0.79
Current	Inverter 1	8.54	8.76	8.49	8.76	8.88	8.54
	Inverter 2	8.54	8.76	8.49	8.76	8.88	8.54

Table 2. Level of over voltage when disturbances occur on the DC line or at the rectifier side during DC block.

TOV for Various RPC's in p.u		Rectifier 1 side 3Φ AC fault		Rectifier 1 side 2Φ AC fault		Rectifier 1 side 1Φ AC fault		Rectifier 1 DC fault	
		Inverter 1	Inverter 2	Inverter 1	Inverter 2	Inverter 1	Inverter 2	Inverter 1	Inverter 2
SC	PI	1.1668	1.1668	1.1432	1.1432	1.1285	1.1285	1.1289	1.1289
	FFPI	1.1349	1.1349	1.1172	1.1172	1.0974	1.0974	1.1045	1.1045
SVC	PI	1.1712	1.1712	1.1502	1.1502	1.1395	1.1395	1.1363	1.1363
	FFPI	1.1405	1.1405	1.1229	1.1229	1.1075	1.1075	1.1101	1.1101
STATCOM	PI	1.0711	1.0711	1.0681	1.0681	1.0494	1.0494	1.0715	1.0715
	FFPI	1.0449	1.0449	1.0421	1.0421	1.0214	1.0214	1.0445	1.0445
FC+SC	PI	1.1469	1.1469	1.1205	1.1205	1.1062	1.1062	1.1092	1.1092
	FFPI	1.1175	1.1175	1.0919	1.0919	1.0781	1.0781	1.0806	1.0806
FC+SVC	PI	1.1553	1.1553	1.1336	1.1336	1.1109	1.1109	1.1196	1.1196
	FFPI	1.1248	1.1248	1.1056	1.1056	1.0799	1.0799	1.0888	1.0888
FC+ STATCOM	PI	1.0565	1.0565	1.0499	1.0499	1.0321	1.0321	1.0524	1.0524
	FFPI	1.0276	1.0276	1.0215	1.0215	1.0088	1.0088	1.0225	1.0225

Table 3. Inverter 1 and 2 DC power recovery time during AC and DC disturbances occur on the rectifier side.

DC power recovery time for Various RPC's in seconds		Rectifier 1 side 3Φ AC fault		Rectifier 1 side 2Φ AC fault		Rectifier 1 side 1Φ AC fault		Rectifier 1 DC fault	
		Inverter 1	Inverter 2	Inverter 1	Inverter 2	Inverter 1	Inverter 2	Inverter 1	Inverter 2
SC	PI	0.085	0.085	0.074	0.074	0.048	0.048	0.344	0.344
	FFPI	0.041	0.041	0.034	0.034	0.019	0.019	0.162	0.162
SVC	PI	0.095	0.095	0.080	0.080	0.055	0.055	0.356	0.356
	FFPI	0.046	0.046	0.039	0.039	0.024	0.024	0.168	0.168
STATCOM	PI	0.080	0.080	0.070	0.070	0.043	0.043	0.332	0.332
	FFPI	0.036	0.036	0.029	0.029	0.016	0.016	0.154	0.154
FC+SC	PI	0.082	0.082	0.072	0.072	0.042	0.042	0.336	0.336
	FFPI	0.038	0.038	0.032	0.032	0.015	0.015	0.157	0.157
FC+SVC	PI	0.090	0.090	0.077	0.077	0.050	0.050	0.0347	0.347
	FFPI	0.042	0.042	0.037	0.037	0.021	0.021	0.161	0.161
FC+ STATCOM	PI	0.074	0.074	0.066	0.066	0.038	0.038	0.324	0.324
	FFPI	0.031	0.031	0.025	0.025	0.013	0.013	0.148	0.148

Table 4. Inverter 1 and 2 DC power recovery time during AC and DC disturbances occur on the inverter side.

DC power recovery time for Various RPC's in seconds		Inverter 1 DC fault		Inverter 1 side 3Φ AC fault		Inverter 1 side 2Φ AC fault		Inverter 1 side 1Φ AC fault	
		Inverter 1	Inverter 2	Inverter 1	Inverter 2	Inverter 1	Inverter 2	Inverter 1	Inverter 2
SC	**PI**	0.349	0.349	0.554	0.554	0.543	0.543	0.532	0.532
	FFPI	0.164	0.164	0.171	0.171	0.168	0.168	0.164	0.164
SVC	**PI**	0.361	0.361	0.566	0.566	0.554	0.554	0.543	0.543
	FFPI	0.171	0.171	0.178	0.178	0.173	0.173	0.167	0.167
STATCOM	**PI**	0.336	0.336	0.541	0.541	0.532	0.532	0.521	0.521
	FFPI	0.156	0.156	0.169	0.169	0.160	0.160	0.154	0.154
FC+SC	**PI**	0.340	0.340	0.548	0.548	0.537	0.537	0.526	0.526
	FFPI	0.160	0.160	0.174	0.174	0.168	0.168	0.162	0.162
FC+SVC	**PI**	0.351	0.351	0.559	0.559	0.546	0.546	0.534	0.534
	FFPI	0.164	0.164	0.177	0.177	0.170	0.170	0.164	0.164
FC+ STATCOM	**PI**	0.329	0.329	0.529	0.529	0.518	0.518	0.506	0.506
	FFPI	0.150	0.150	0.163	0.163	0.148	0.148	0.143	0.143

4.1. Inverter Side AC Harmonics

The inverter side AC voltage and current waveforms and their harmonic spectrums during steady state operation are presented in Figures 5, 6 and the results are listed in Table 1. From the inverter side AC waveforms and their harmonic spectrum, it is clear that in all the cases the voltage and current are equal to 1p.u and the harmonics are within tolerable limit. The 11^{th} and 13^{th} current harmonics are the foremost harmonics on the inverter AC side.

4.2. Temporary overvoltage

When disturbances occur on the DC line or at the rectifier side, commonly temporary over voltage happens. It is usual practice a large number RLC based filters are provided in the inverter side of the HVDC system, in order to supply the part of necessary reactive power. During rectifier side AC or DC faults (the inverter side has no faults), the DC is blocked, and hence the reactive power of those filters will flow into the AC system, which often causes TOV. In order to suppress the TOV, the reactive power compensator and DC system PI controllers should respond quickly otherwise the TOV could be very high and could damage the insulation of the equipment. The ability of TOV suppression of various RPC's is demonstrated with the proposed firefly algorithm based PI controller and also compared to a conventional PI controller. From the inverter side RMS AC voltage waveforms presented in Figures 7, 8 and the results listed in Table 2, the existence of TOV in the presence of a conventional PI controller for various RPC's can be understood. The hybrid RPC's (FC+SC, FC+SVC and FC+STATCOM) has enhanced TOV controlling capability, than their individual performance (SC, SVC and STATCOM). In particular, FC+STATCOM have a smaller amount of TOV among the various RPC's. The TOV values further reduced due to the application firefly algorithm based PI controller compared to conventional PI controller.

4.3. Fault Recovery

The time taken by the HVDC system to recover the 80% of the pre-fault power after the fault clearance is known as DC power recovery time. The DC power recovery time is often desired the recovery ability of a DC system PI controller and the capability of the RPC's during system disturbances. From the inverter DC power recovery simulation results (Figures 9, 10, 11, 12 and Table 3, 4), it is observed that in all the cases during rectifier side AC system faults, the system recovery with the firefly algorithm based PI controller is considerably faster than the conventional PI controller. On the other hand, for the faults in the rectifier DC side and inverter AC and DC side, the hybrid RPC's (FC+SC, FC+SVC and FC+STATCOM) has reduced fault clearing time than their individual performance (SC, SVC, and STATCOM). Specifically, the mixture of FC and STATCOM

is taking much reduced time to clear the fault among the various RPC's. Further, the firefly algorithm based PI controller makes the system recovery much quicker than the conventional PI controller.

V. CONCLUSION

In this paper, an in depth performance analysis of a multi-terminal LCC-HVDC system feeding weak AC networks was carried out with hybrid RPC's and firefly algorithm based optimal PI controller for rectifiers and inverters control. The various hybrid RPC's considered were FC+SC, FC+SVC and FC+STATCOM. This involvement can be very useful for designing and safeguarding persons, for analyzing the interaction between AC networks and HVDC systems under different operating environment. The HVDC transmission system model was simulated using Matlab software. The transient performances of the hybrid RPC's in an HVDC system were compared with SC, SVC, STATCOM under various fault condition to study the suppression of TOV and fault recovery. The simulation results authenticate that the equal combination of FC+STATCOM has the steady and fastest response and display the superiority of firefly algorithm based PI controller over the conventional fixed gain PI controller. The harmonic analysis result also guarantees the quality of power supply at inverter AC side.

VI. FUTURE WORKS

The analysis done in this paper may be extended to real large power system, in which HVDC links are embedded in a large AC network with proper combination of reactive power compensators at inverter AC side together with an economic assessment to achieve an optimal technical performance with minimal cost.

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AUTHORS

S. Singaravelu received Bachelor of Engineering in Electrical and Electronics in 1990, Master of Engineering in Power System in 1992 and Ph.D. in 2007 from Annamalai University, Annamalainagar, Tamilnadu, India. At Present, he is a Professor in the Department of Electrical Engineering at Annamalai University. His research interests are in power electronics, power systems, electrical machines, wind/solar energy applications, high voltage DC transmission and smart grids.

S. Seenivasan received Bachelor of Engineering in Electrical and Electronics in 2005 and Master of Engineering in Power System in 2011 from Annamalai University, Annamalainagar, Tamilnadu, India. He is currently pursuing Ph.D. degree in the Department of Electrical Engineering, Annamalai University. At present, he is an Assistant Professor in the Department of Electrical Engineering at Annamalai University. His research interests are in high voltage DC transmission systems and soft computing techniques.